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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,114	07/09/2003	Thomas Hanuschek	P2002,0587	2189

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EXAMINER	
TRUONG, LOAN	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/616,114	HANUSCHEK ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *December 22, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination filed December 22, 2006 in application 10/616,114.

2. Claims 1-8 are presented for examination. Claims 1 and 5 have been amended.

Response to Arguments

3. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemasa et al. (US 6,981,179) in further view of Sim et al. (US 6,990,607).

In regard to claim 1, Shigemasa et al. teach an integrated module, comprising:

an external access terminal (*microcomputer is connected to an external communication device and a control computer, fig. 1, 10, 20, 30)*;

a memory including memory cells for storing code (*boot ROM, fig. 1, 16)* and data (*nonvolatile memory, RAM, fig. 1, 11, 12)*;

a microcontroller (*microcomputer, fig. 1, 10)* connected to said external access terminal (*external communication device, fig. 1, 20)* and to said memory (*ROM, RAM, nonvolatile memory, fig. 1, 11, 12, 16)*, said microcontroller (*microcomputer, fig. 1, 10)* controlling an access (*test program is stored in the RAM and run by the CPU to conduct a check-up of the nonvolatile memory, col. 5 lines 58-61)* to said memory (*nonvolatile memory, fig. 1, 11)* and a data transfer through said external access terminal during normal operation (*test program is transfer to the RAM from the external communication device, col. 5 lines 58-61)*, said microcontroller (*microcomputer, fig. 1, 10)* controlling a performance of a test sequence (*test program is run by the CPU to conduct a check-up of the nonvolatile memory, fig. 1, 13, col. 5 lines 58-61)* said memory in a test operation of the module (*nonvolatile memory, fig. 1, 11)*; and

Shigemasa et al. does not explicitly teach the module comprising of a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing, said addresses being stored in said defect data memory under control of said microcontroller.

Sim et al. teach the system for adaptive storage and caching of a defect table by implementing the defect table (*fig. 3, fig. 4, 430, paragraph 0048)* to disclosed the index,

head, cylinder, sector and span of the defect location *(fig. 3),* the defect table in a mass storage device with a microcontroller operably coupled to the recording medium that stores the defect table *(fig. 4, 410, 430, 440, paragraph 0048).*

It would have been obvious to modify the module of Shigemasa et al. by adding Sim et al. defect table. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would enables a defect table that is adaptive and dynamic in size, capacity and/or length and also provide the defect table to be stored in a manner that reduces seek time between the regions of data and the defect table *(paragraph 0014).*

In regard to claim 2, Shigemasa et al. disclosed the integrated module according to claim 1, further comprising a command memory for storing *(Test program are stored in the RAM, col. 5 lines 58-61)* an externally supplied command sequence *(test program transfer from the external communication device, col. 5 lines 58-61)* and on a basis of the command sequence said microcontroller controls a carrying out of the test sequence *(CPU run the test program transferred from the external communication device, col. 5 lines 58-61).*

In regard to claim 3, Shigemasa et al. does not explicitly teach the integrated module according to claim 1, wherein said defect data memory is part of said microcontroller.

Sim et al. teach the system for adaptive storage and caching of a defect table with the volatile memory of the microcontroller containing the defect buffer *(fig. 4, 440, 450, 460).*

Refer to claim 1 for motivational statement.

In regard to claim 4, Shigemasa et al. disclosed the integrated module according to claim 2, wherein said command memory is part of said microcontroller (*microcontroller comprises a RAM that stored the test program transferred from the external communication device, col. 5 lines 33-37 and lines 58-61).*

In regard to claim 5, Shigemasa et al. disclosed a method for functionally checking a memory of an integrated module, which comprises the steps of:

reading-in a command sequence externally before beginning a test operation (*the external communication device sends a signal (command) to the I/O terminal of the microcomputer to start transfer of the test program, col. 7 lines 16-23)*, and on a basis of the command sequence a microcontroller controls a carrying out of a test sequence (*microcomputer sets the conditions necessary for the transfer and stores the received test program in the RAM, col. 7 lines 16-29)*

executing the command sequence for carrying out the test sequence by the microcontroller (*CPU confirms the completion of the transfer of the test program and switches the control onto a specific address in the RAM area to starts to run the test program on the RAM, col. 7 lines 30-39)*; and

Shigemasa et al. does not explicitly teach the storing addresses of memory cells of the memory which have been detected as defective during the functional testing in a defect data memory, said addresses being stored in said defect data memory under control of said microcontroller.

Sim et al. teach the system for adaptive storage and caching of a defect table by implementing the defect table *(fig. 3, fig. 4, 430, paragraph 0048)* to disclosed the index, head, cylinder, sector and span of the defect location *(fig. 3),* the defect table in a mass storage device with a microcontroller operably coupled to the recording medium that stores the defect table *(fig. 4, 410, 430, 440, paragraph 0048).*

Refer to claim 1 for motivational statement.

In regard to claim 6, Shigemasa et al. disclosed the method according to claim 5, which further comprises:

making a jump to a start address in an internal command memory after the command sequence is read-in at the beginning of the test operation (*CPU switches the control onto a specific address in the RAM area, col. 7 lines 30-36)*;

executing the command sequence under the control of the microcontroller proceeding from the start address (*CPU switches the control onto a specific address in the RAM area and starts to run the test program, col. 7 lines 30-36)*;

Shigemasa et al. does not explicitly teach the method of storing the addresses of the memory cells of the memory which have been detected as defective during functional testing generated in the defect data memory under the control of the microcontroller; and reading-out the addresses of the memory cells of the memory which have been detected as defective during functional testing stored in the defect data memory, under the control of the microcontroller, to outside the integrated module for further evaluation.

Sim et al. teach the system for adaptive storage and caching of a defect table by implementing the defect table *(fig. 3, fig. 4, 430, paragraph 0048)* to disclosed the index, head, cylinder, sector and span of the defect location *(fig. 3)*, the defect table in a mass storage device with a microcontroller operably coupled to the recording medium that stores the defect table *(fig. 4, 410, 430, 440, paragraph 0048)*. Furthermore, a segment of the defect table is copied to a volatile memory device of the mass storage table by a determination of the most recently used entries *(fig. 6, 600, paragraph 0056)*.

Refer to claim 1 for motivational statement.

In regard to claim 8, Shigemasa et al. does not teach the integrated module according to claim 1, wherein the microcontroller is embodied as a hard disk controller.

Sim et al. teach the system for adaptive storage and caching of a defect table on a disk drive such as a magnetic disc drive *(fig. 19)*.

Refer to claim 1 for motivational statement.

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5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemasa et al. (US 6,981,179) in further view of Sim et al. (US 6,990,607) in further view of Suzuki et al. (US 2002/0066056).

In regard to claim 7, Shigemasa et al. and Sim et al. does not teach integrated module according to claim 1, wherein said defect data memory and said command memory are part of a dual-port RAM.

Suzuki et al. disclosed the method of testing semiconductor memory by having a dual-port RAM with one port for suppling data while the other port supplied with feedback data from data operation *(fig. 5, paragraph 0062)*.

It would have been obvious to modify the module of Rajsuman et al. and Dahn by adding Suzuki et al. method of testing semiconductor memory by having a dual-port RAM. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide optimum data for detecting a defect difficult to be detected by the regular test pattern *(paragraph 0064)*.

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER